



AMENDMENTS TO THE DRAWINGS

Please replace drawing sheet for Fig. 6a with the enclosed replacement sheet.

REMARKS

Claims 1, 2 and 4-23 are currently pending in the subject application and are presently under consideration. Applicant's representative acknowledges with appreciation the indication of claims 5 and 6 as being allowable subject to being re-written in independent form and reciting limitations of the base claim and any intervening claims. It is believed such amendments are not necessary at the present time in view of the deficiencies discussed *infra* regarding the cited reference, Mandell *et al.* However, applicant's representative reserves the option to recast such claims at a later date if necessary

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Objection to Drawings

The drawings are objected to because of minor informalities. Applicant's representative has amended Fig. 6a (removal of reference numerals 110, 220) – a replacement sheet for such figure is provided herein. No new matter has been added.

Moreover, it is respectfully submitted that the drawings properly show features of claim 8, (*e.g.*, Fig. 6a electrode components A, B, C), and a detailed illustration of the read and write circuits is not essential for a proper understanding of the invention. Withdrawal of this objection is respectfully requested.

II. Objection of Claims 1, 7 and 12

Claims 1, 7 and 12 are objected to because of minor informalities. Withdrawal of such objection is respectfully requested, as proper antecedent basis is provided for claim elements. For example, contrary to assertions made in the Office Action, proper antecedent basis for the term "property" is provided in claim 1- (*See* claim 1: "a control component that applies an external stimulus to the memory cell, to affect *a property* [...]").

Likewise, proper antecedent basis is provided in claim 12 for the term "the comparing act"- such claim depends from independent claim 9 that recites "*comparing* the impedance state with a predetermined threshold value". Moreover, elements of claim 7 such as the passive layer, active layer and barrier layer are adequately defined in the Specification (*See* Specification at p. 10 and p.18, for example.)

III. Rejection of Claims 1, 2, 4 and 7-23 Under 35 U.S.C. §103(a)

Claims 1, 2, 4 and 7-23 stand rejected under 35 U.S.C. §103(a) as being obvious over Mandell *et al.* (US Patent 6,627,944). Withdrawal of this rejection is respectfully requested for at least the following reasons. Mandell *et al.* does not disclose the claimed invention.

To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the Applicant's disclosure. See In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

The subject invention as claimed relates to programming semiconductor memory device(s) having a functional layer that is sandwiched between a *first electrode* and a *second electrode*. Changes of an impedance state of the functional layer located between such *electrodes* is indicative of information content. Such aspects of the claimed invention are not taught by Mandell *et al.* Mandell *et al.* is directed to a floating gate memory where a *first insulating layer* is provided underneath a floating gate and a *second insulating layer* is provided over the floating gate. (See column 2 lines 1-4 of Mandell *et al.* that recites; “A floating gate is provided on the first *insulating layer*, and a *second insulating layer* is on the floating gate.”) Thus, a floating gate is sandwiched *between insulating layers*— not a functional layer sandwiched between *electrodes* as in the subject invention.

Moreover, contrary to the assertions made in the Office Action, Mandell *et al.* does not require a control mechanism to determine a program state, because the floating gate of Mandell *et al.* is automatically discharged upon the insulating layer reaching a threshold conductive state. Hence, contrary to assertions made in the office Action, no comparator is required to determine a program state, as recited in independent claim 1.

Similarly, since in Mandell *et al.* upon reaching a threshold conductive state discharge occurs, there exists no motivation to supply a diode that introduces *another break down voltage*, as recited in claims 18-21.

In view of the at least above comments, it is readily apparent that Mandell *et al.* does not make obvious applicant's invention as recited in the subject claims, and this rejection should be withdrawn.

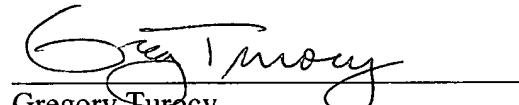
CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP1027US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,
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